Cpk Based Variation Reduction: 14nm FinFET Technology

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GLOBALFOUNDRIES®

Outline

- Background: Cpk methodology
- Specification Verification
  - Methodology
  - Structural simulation
  - Physical parameter regression
  - Electrical to physical parameter regression
- Case study
  - Gate Height control

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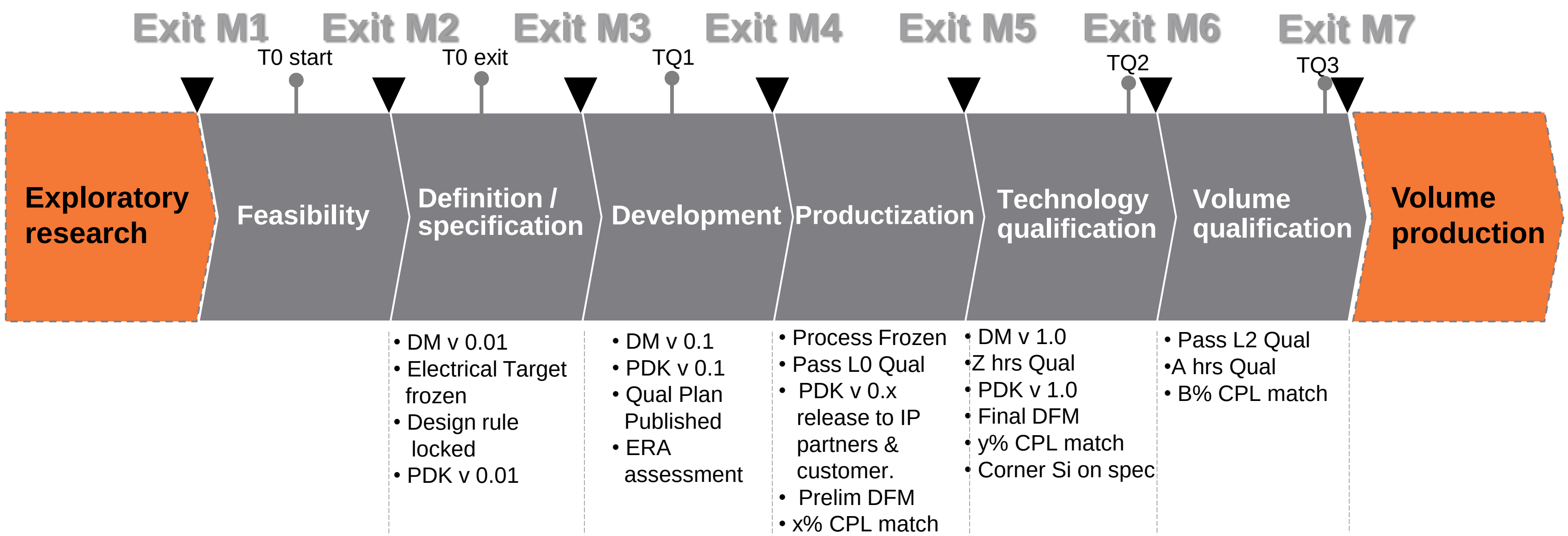
Technology Development Roadmap



- There are pre-determined Milestones for a technology to go from Research to Volume production.
- These milestones measure the maturity of the technology using performance, yield, reliability, and variation metrics.
- Maturity for each of these attributes is key to deliver a competitive product at that technology.

Capability indices

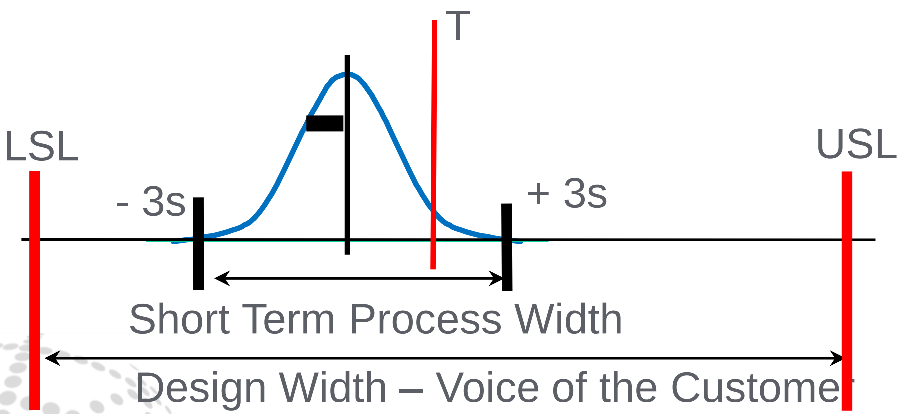
Capability indices (k, Cp, Cpk) are commonly used to assess the variation maturity of a technology and product.

$$C_p = \frac{(USL - LSL)}{6\sigma}$$

$$C_{pk(USL)} = \frac{(USL - \mu)}{3\sigma}$$

$$C_{pk} = \text{Min}\{C_{pk(USL)}, C_{pk(LSL)}\}$$

$$C_{pk(LSL)} = \frac{(\mu - LSL)}{3\sigma}$$

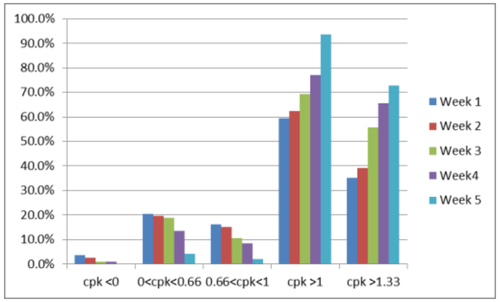


C_{pk}	Sigma level (σ)	Process yield	Parts defective (PPM)
0.33	1	68.27%	317311
0.67	2	95.45%	45500
1	3	99.73%	2700
1.33	4	99.99%	63
1.67	5	100.00%	1
2	6	100.00%	0.002

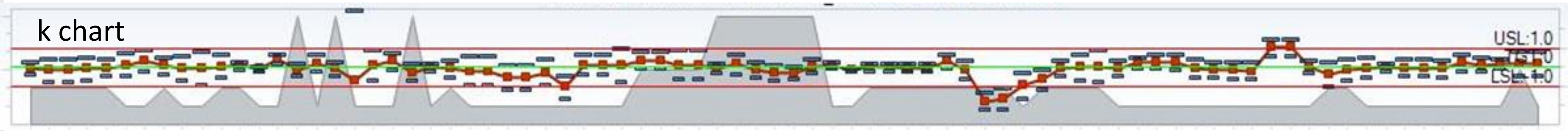
Cpk based process improvement

- <u>Advantages</u>
  - Cpk provides an easy to track metric to assess variation improvement for a technology.
  - K charts provide easy visualization of areas of concern.
  - Cpk maturity level (e.g. 90% parameters with Cpk > 1.33) is a gating item for technology milestone achievement.

Cpk tracking



k chart



- <u>Disadvantages</u>
  - Cpk is a strong function of the specification limits.
  - How do we determine the specification limits?
    - For technology in pathfinding phase
    - For technology in development
    - For technology in ramp
    - For technology in volume production

$$C_p = \frac{(USL - LSL)}{6\sigma}$$

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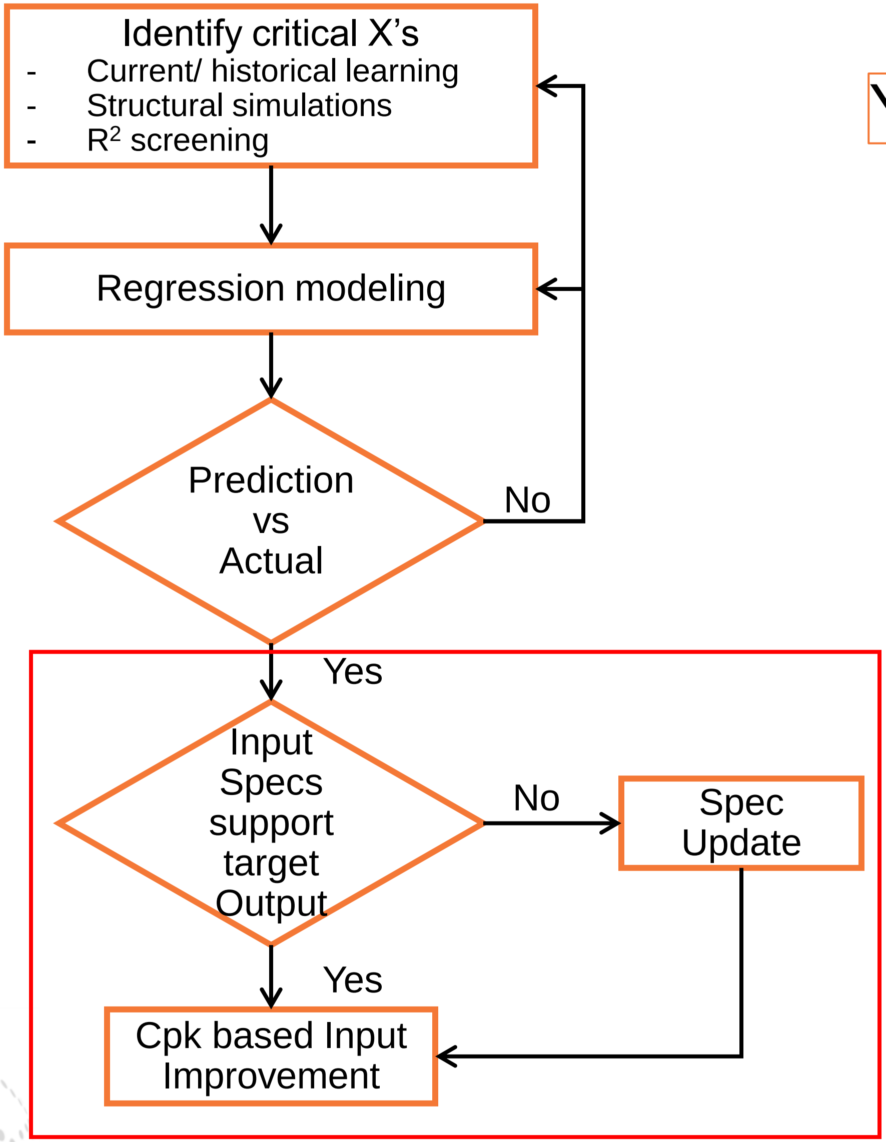
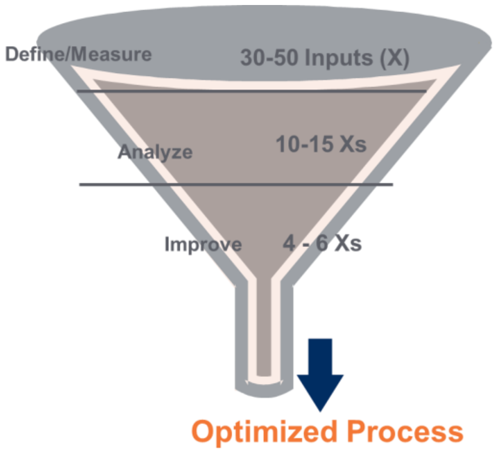
Methodology



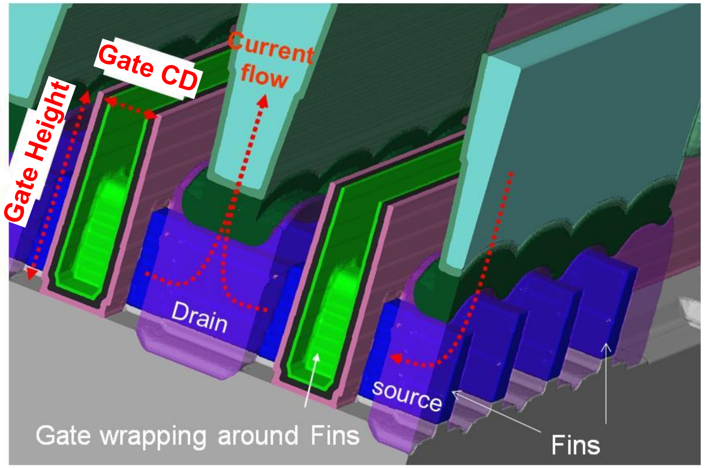
$Y = f(X_i)$ Y = output, X_i = inputs

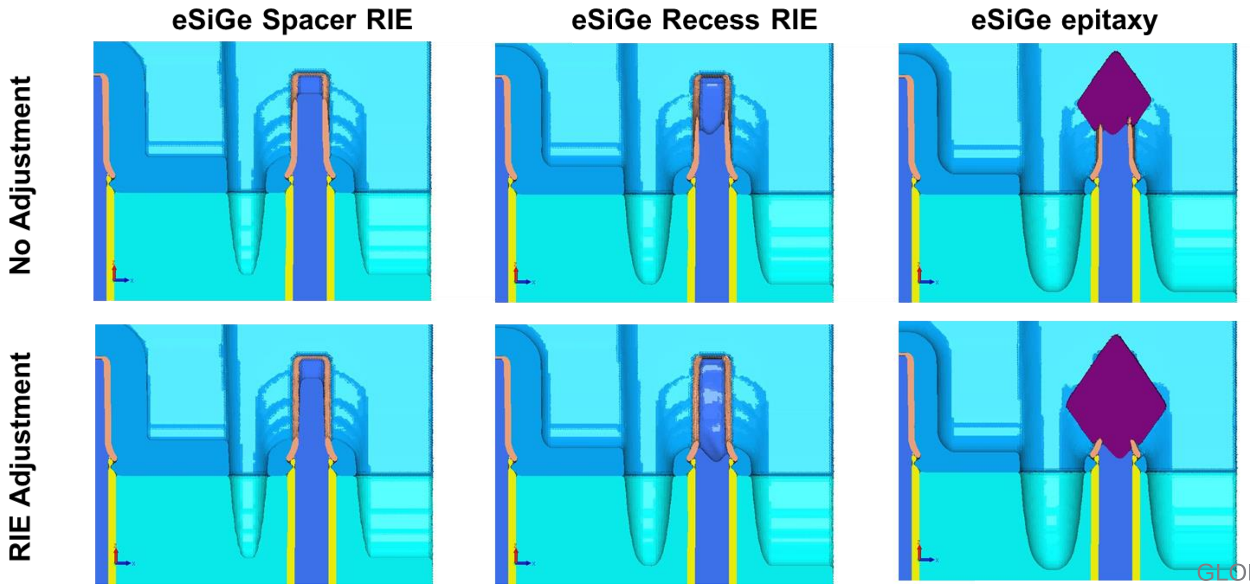
DMAIC methodology



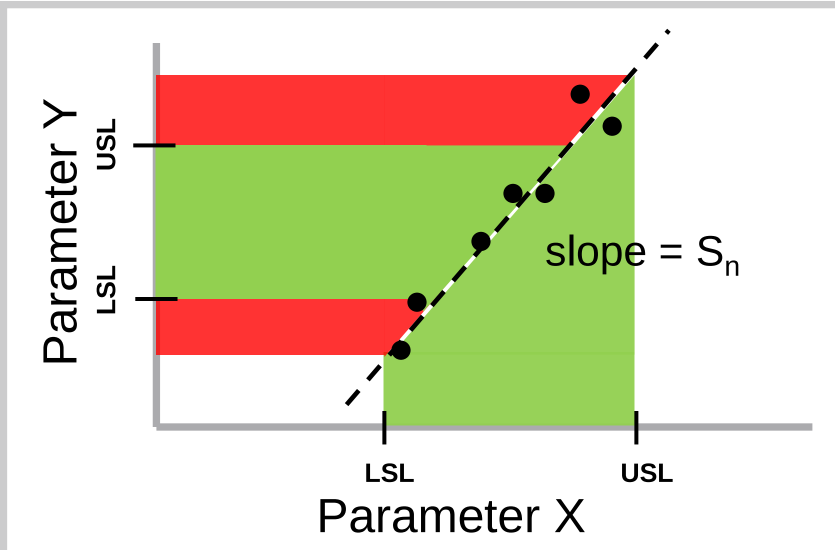
Structural simulations

- FinFET technologies
  - Deviation from standard planar device architecture
  - Significant increase in processing complexity.
- Structural simulations employed
  - Design rule and process marginality check
  - Assess knock-on effect of process changes
  - Screening DOEs





Physical parameter regression



- Linear regression fit of parameters X and Y with slope $S_{(n)}$

$$Y = C + S_{(n)} X$$

- Criteria for spec validation would be

$$[USL(Y)- LSL(Y)] <= S_{(n)} [USL(X)- LSL(X)]$$

	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15
P1	1.00	0.63	0.00	0.23	0.00	0.46	0.24	0.05	0.42	0.09	0.40	0.94	0.12	0.46	0.83
P2	0.30	1.00	0.00	0.00	0.01	0.04	0.07	0.39	0.00	0.00	1.00	0.71	0.00	0.37	0.00
P3	0.00	0.98	1.00	0.03	0.27	0.67	0.00	0.00	0.64	0.00	0.37	0.00	0.35	0.19	0.00
P4	0.30	0.00	0.43	1.00	0.94	0.17	0.53	0.00	0.00	0.00	0.00	0.59	0.94	0.13	0.05
P5	0.00	0.00	0.29	0.63	1.00	0.18	0.26	0.31	0.14	0.00	0.00	0.00	0.36	0.72	0.22
P6	0.20	0.32	0.30	0.20	0.00	1.00	0.53	0.14	0.00	0.28	0.00	0.83	0.08	0.00	0.41
P7	0.00	0.31	0.41	0.11	[illegible]	0.00	1.00	0.00	0.00	[illegible]	0.00	0.23	0.19	0.00	0.00
P8	0.34	0.54	0.27	0.00	[illegible]	0.00	0.01	1.00	0.33	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	0.57
P9	0.28	0.77	0.66	0.30	[illegible]	0.01	0.00	0.00	1.00	0.00	[illegible]	[illegible]	[illegible]	0.34	0.00
P10	0.09	0.80	0.19	0.21	[illegible]	0.22	0.55	0.00	0.04	1.00	0.00	0.00	0.18	[illegible]	0.00
P11	0.00	0.54	0.00	0.95	0.00	0.18	0.00	0.64	0.00	0.00	1.00	0.09	0.00	[illegible]	0.00
P12	0.00	0.00	0.00	0.00	0.00	0.33	0.03	0.26	0.00	0.00	0.01	1.00	0.48	[illegible]	0.00
P13	0.02	0.11	0.00	[illegible]	[illegible]	[illegible]	0.81	0.14	0.00	0.00	0.23	0.00	1.00	[illegible]	0.00
P14	0.11	0.59	0.81	[illegible]	[illegible]	[illegible]	[illegible]	0.00	0.78	0.80	0.02	0.00	0.00	[illegible]	0.54
P15	0.00	0.00	0.00	0.69	0.00	0.00	0.00	0.00	0.97	0.11	0.41	0.14	0.00	0.70	1.00

Influencing process

Impacted process

	P2		Spec validation
P2	1.00	High Correlation > 0.7	Yes
P3	0.98		Yes
P10	0.80		No
P9	0.77		Yes
P1	0.63	Ver Low & Med significant Correlation 0 < r < 0.69	N/A
P14	0.59		N/A
P11	0.54		N/A
P8	0.54		N/A
P6	0.32		N/A
P7	0.31		N/A
P13	0.11		N/A
P4	0.00		N/A
P5	0.00		N/A
P12	0.00		N/A
P15	0.00		N/A

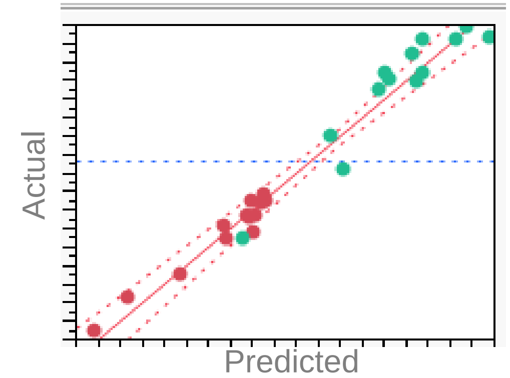
Electrical to physical parameter regression

Physical measurement

ET measurement

	0.040		0.003		0.006	0.133
	0.133		0.004		0.000	0.243
			0.034		0.125	0.023
			0.458		0.216	0.217
			0.099		0.301	0.000
			0.209		0.091	0.076
0.225	0.322	0.283	0.436		0.497	0.102
0.926	0.010	0.210	0.509		0.864	0.398
	0.591	0.566	0.730	0.518	0.774	0.709
	0.591	0.545	0.707	0.178	0.782	0.799
0.061	0.042	0.049		0.219	0.334	0.063
	0.307	0.285	0.004		0.153	0.019
	0.338	0.282	0.058		0.259	0.085
	0.684	0.418	0.407		0.444	0.131
	0.595	0.301	0.350		0.556	0.067
	0.342	0.134	0.161		0.011	0.001
	0.663	0.099	0.513		0.640	0.182
	0.573	0.532	0.696	0.052	0.751	0.789
		0.595	0.729	0.430	0.765	0.820
		0.545	0.490	0.173	0.398	0.717
	0.001	0.414	0.345	0.078	0.411	0.067
		0.609	0.591	0.330	0.589	0.058
		0.000	0.004	0.002	0.513	0.141
0.225	0.001	0.123		0.441	0.255	0.245
0.706	0.233	0.235	0.325	0.206	0.527	0.168
0.363	0.346	0.275		0.322	0.445	0.052
	0.145	0.230			0.610	0.017

R2 screening for critical physical parameters



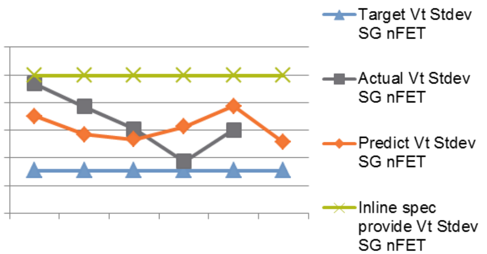
Modeling using stepwise regression/ principal component analysis

Physical measurement

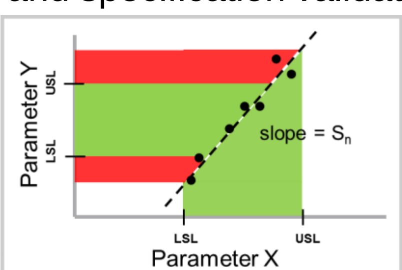
ET measurement

-0.01247	0.000191	-0.00532	0.0014398
0.002917	-0.00316	0	-0.015927
		0.0138	0.0166
0.035446	-0.00931	0.016196	0.011795
		0.02149	0.0348
0.004494	0.001571	0.035411	-0.054
0.033457	-0.01258		
0.152424	-0.05053		

Determination of ET to physical sensitivities



Model and specification validation



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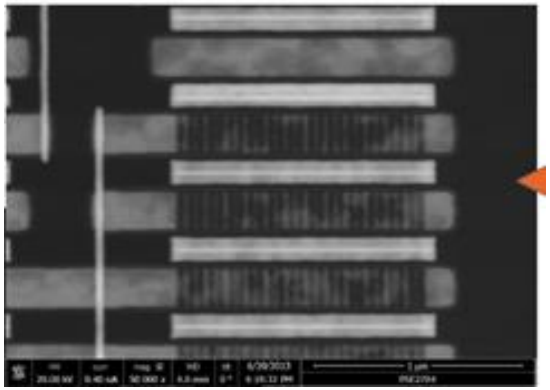
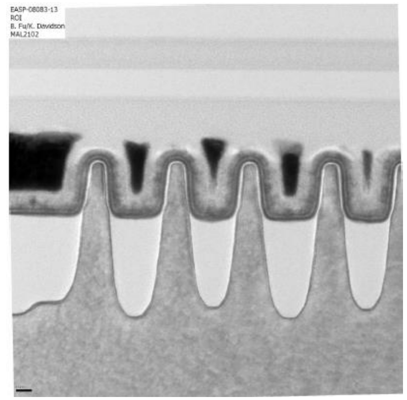
Gate Height Issue





Problem: Insufficient gate height was identified as a key issue for yield and device step-up.

Gate height for a FinFET/ RMG technology is influenced by many steps.

Fin definition

Dummy poly definition

Junction eSiGe + eSiP

Poly Open

Gate oxide patterning

Work function patterning

W fill & W CMP

W RIE and SAC CMP

Gate height improvement

Identify the key inline parameters → Define Specification limits → Improve Cpk

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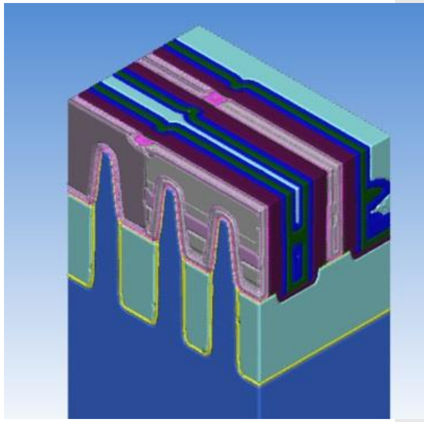
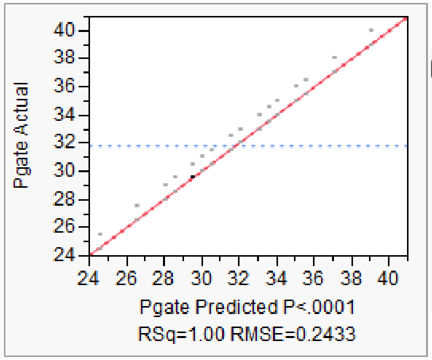


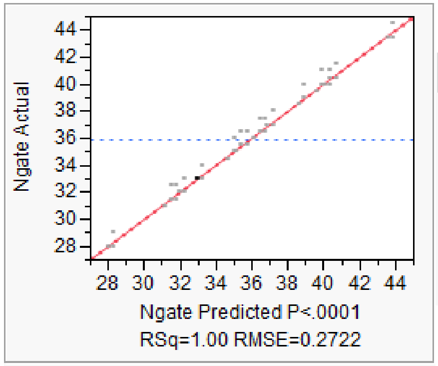
- A 9 factor two level DOE was executed for structural simulation.

  - Based on the simulation Fin reveal, Poly CMP, Poly Open CMP, and W CMP were statistically significant.



Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Intercept	31.8125	0.01075	2959.2	<.0001*
Fin Reveal(35,40)	1	0.01075	93.02	<.0001*
Poly Buff(30,35)	-2.5	0.01075	-232.6	<.0001*
Poly Open(4,8)	-2	0.01075	-186.0	<.0001*
W CMP(3,6)	-1.75	0.01075	-162.8	<.0001*



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Gate height improvement

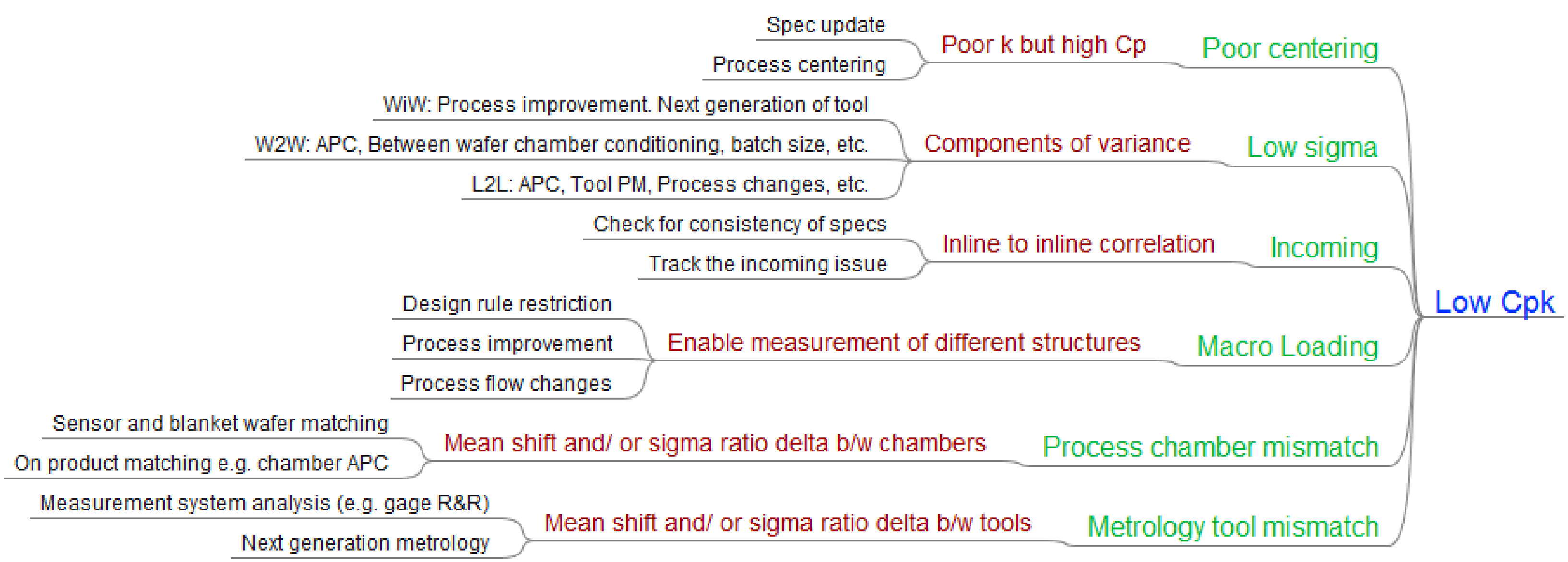
Identify the key inline parameters → **Define Specification limits** → Improve Cpk

- Specification limits were defined to support a final gate height variation of +/-10nm as the first step.
- Sigma target was assigned to each of the contributing steps.
- Root mean square of variances from the contributing steps were used to include the incoming variation for specification limits determination.
- The final targeting was based on yield and ET performance.

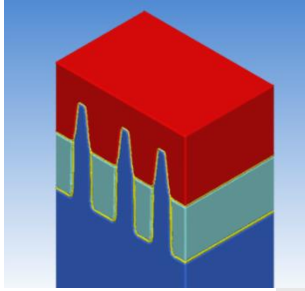
	Step 1 (6sigma, nm): Original Step 1 proposal	
	6 sigma	Proposed SPEC (USL-LSL)
Target (total variation) ->	20	
WCMP	8	20.0
POC	8	17.0
Poly height post CMP	10	10
Performance (RMS)->	19.8	

Gate height improvement

Identify the key inline parameters → Define Specification limits → **Improve Cpk**

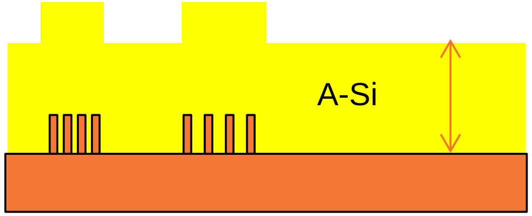


Poly CMP improvement

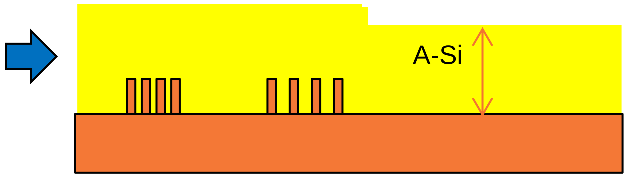


POR

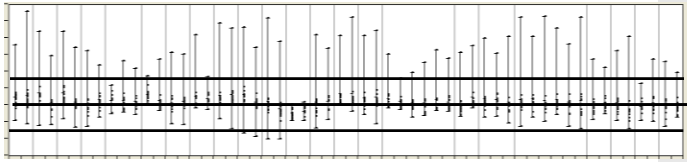
a-Si Dep

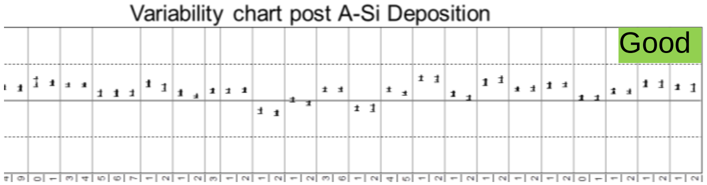


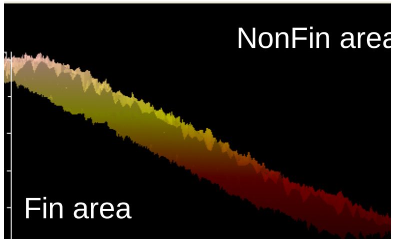
a-Si CMP



Cpk ~ 0.4, Spec +/-8nm



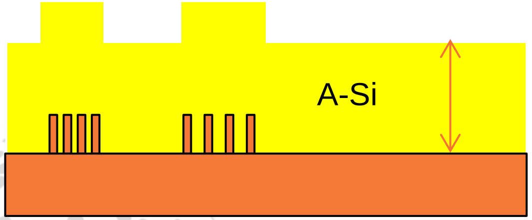




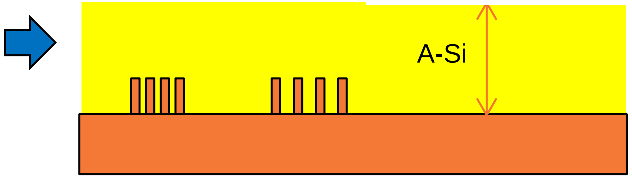
aSi height delta between Fin/ non Fin area and within wafer variation and are the main sources of variation.

Go To

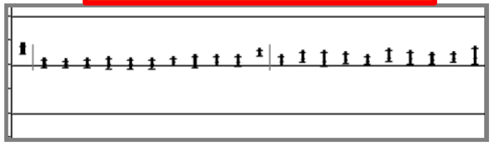
a-Si Dep



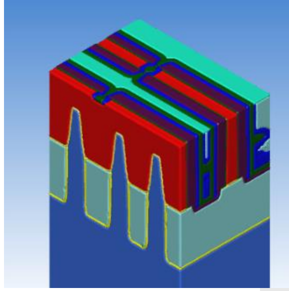
Planarization improvement



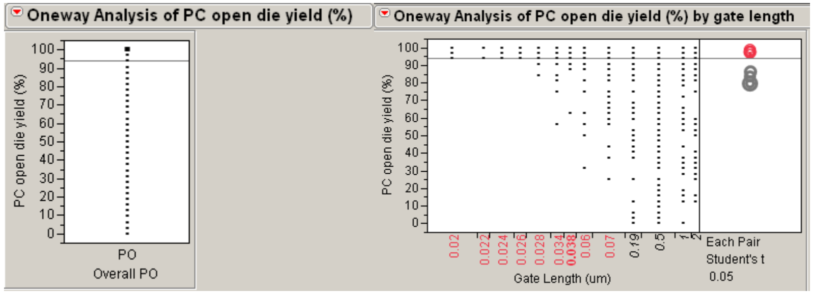
Cpk ~ 3.6, Spec +/- 5nm

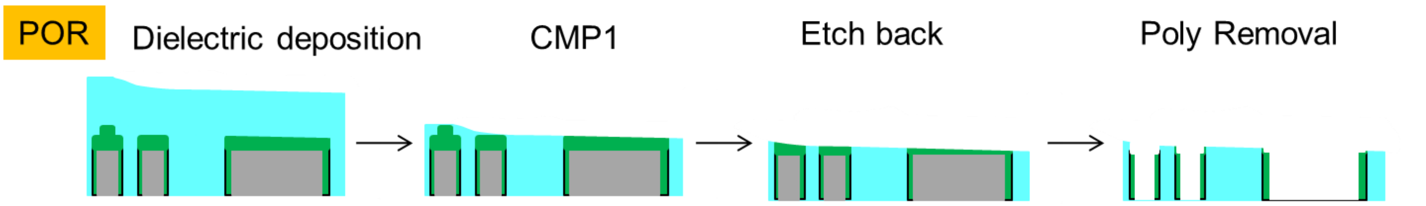


Poly Open improvement

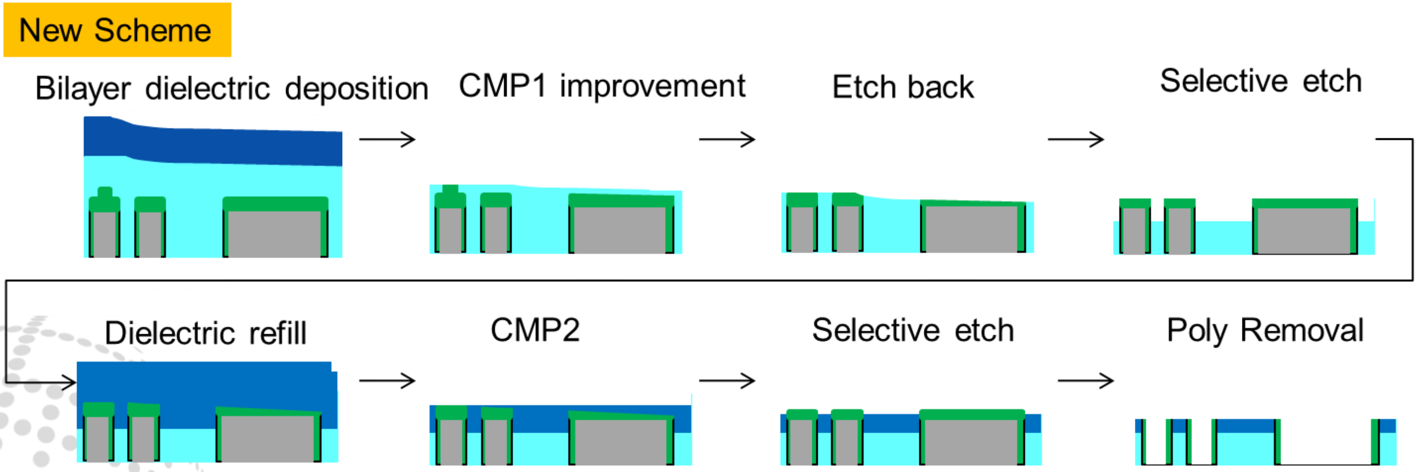


- PC open yield varies from 0 to 100%
- From Anova test, long channel PC open yield statistically showed degrading from 190nm PC open yield data indicating shorter gate height for longer channel macros – **impact from loading effect**



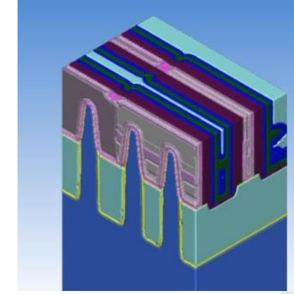


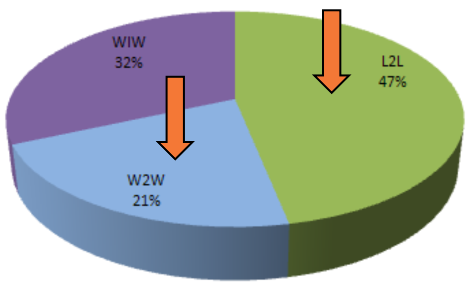
POR process capability
Aleris: C_{pk}= 0.91
OCD: C_{pk}= 0.36



New process capability
Aleris C_{pk}= 1.47
OCD: C_{pk}= 1.1

W CMP improvement





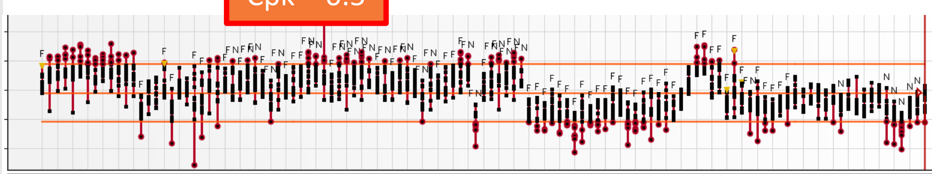
BEFORE

W depostion

W CMP by fix time

W RIE

Cpk ~ 0.5



AFTER

W Deposition

Feed forward incoming THK

W CMP: APC controlled

Feed back polish rate

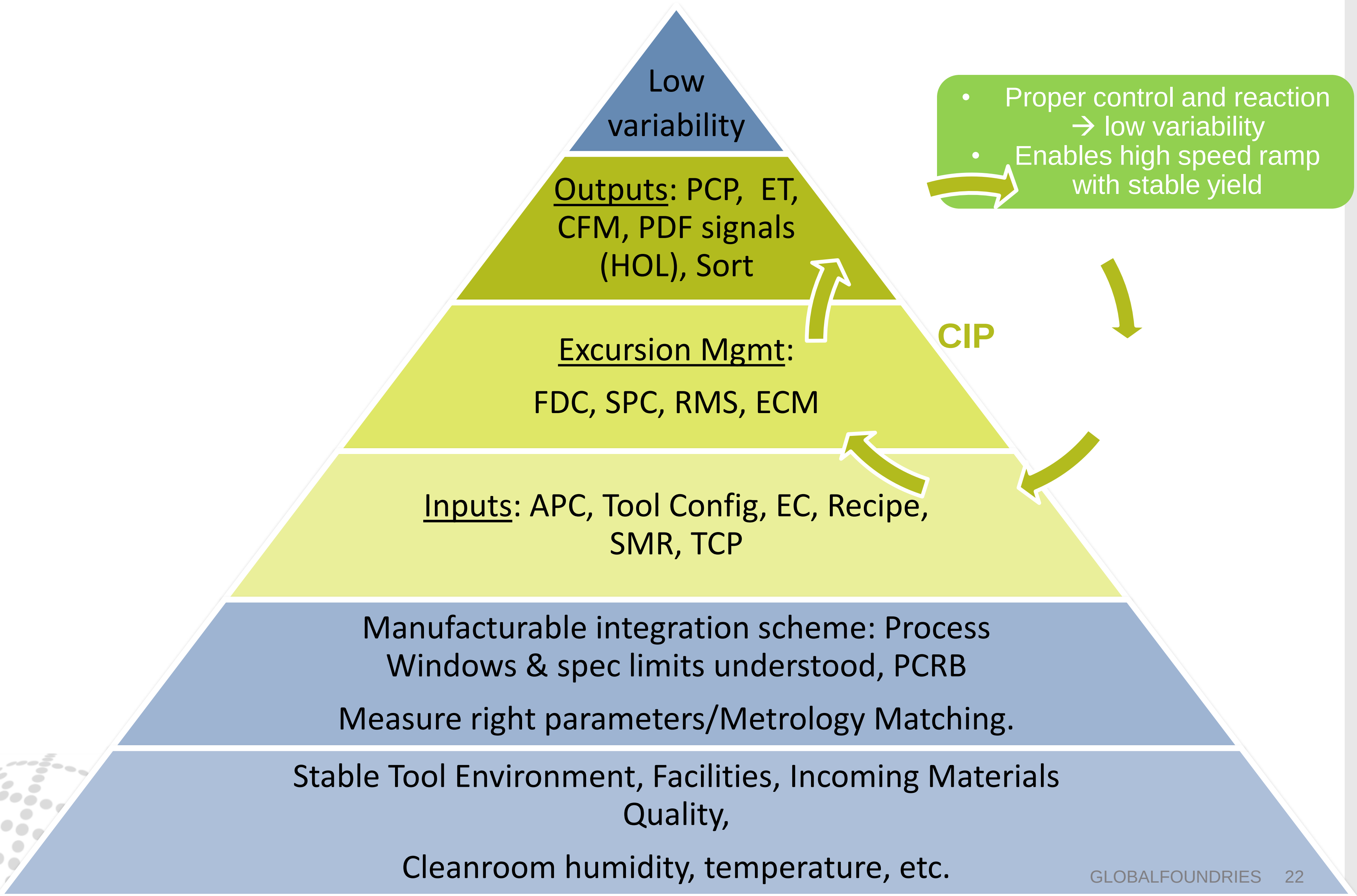
W RIE

Cpk ~ 1

Conclusions

- Capability indices (k, Cp, Cpk) are commonly used to assess the variation maturity of a technology and product.
- Normalization to specification limits in Cpk calculation requires all specification limits to be consistent with the required performance of the final product.
- Improving variation of a key output involves identification of the critical inputs as well as determination of the correct specifications limits to support the desired variation.
- Structural simulations and physical to physical, electrical, and yield correlations were used to define specifications limits for physical measurements.
- Gate height variation improvements for 14nm FinFET technology was demonstrated using this methodology.

GLOBALFOUNDRIES variation reduction



Thank you!

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